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EXAMINER
NGUYEN, HIEP

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,679	MAGOON ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,7,9 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7,9 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Applicant's amendment filed on 12-04-02 has been received and entered in the case. New ground of rejections necessitated by the amendment is set forth below.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 3, 6, 9 and 10 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In this instant, the specification fails to describe as to how " the impedance circuit configured with a sufficiently high impedance to reduce the parasitic capacitance between the first terminal and the second terminal of the transistor by preventing the third switch node from functioning as an alternating current ground during operation of the switch" in claim 1, "the inverter circuit configured to **reduce parasitic effects** at the **first terminal** when **the transistor circuit functions as an open circuit by providing a voltage to the second terminal** when the control signal engages the transistor device" in claim 3, "the third transistor device configured with predetermined parasitic characteristics that improve the effective parasitic characteristics of the transistor circuit" in claim 6, the limitations of claim 9 and claim 10. Discussion of the parasitic capacitance and parasitic effects are seen throughout pages 7-13 of the specification. However, none of the discussion demonstrates the reduction in parasitic capacitance or as to how the parasitic capacitance or the parasitic effects being reduced as recited in claims 1, 3, 6, 9 and 10. Claims 2, 4 and 7 are also rejected under 35 U.S.C. 102 , 1st paragraph because of the technical deficiencies of claims 1, 3 and 6.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/ or clarification is required.

Regarding claim 1, the recitation "the **impedance circuit** configured with a sufficiently high impedance **to reduce the parasitic capacitance** between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current ground during operation of the switch" is indefinite because it is misdescriptive. It is well known in the art that all junction type devices, including transistors, have intrinsic capacitance loading between various junctions commonly referred to as parasitic capacitance thus, the **parasitic capacitance is a fixed value** that **cannot be changed or reduced**. The effect of the parasitic capacitor, however can only be **compensated** by incorporating an input circuit with sufficient high impedance that provide low droop rate. The same analysis is true for the recitation " to reduce" on line 10 of claim 3, line 2 of claim 10.

Regarding claim 3, the recitation "the inverter circuit configured to **reduce parasitic effects** at the **first terminal** when **the transistor circuit functions as an open circuit by providing a voltage to the second terminal** when the control signal engages the transistor device" is indefinite because it is not clear how the parasitic effect at the **first terminal** can be reduced when the "**transistor circuit**" functions as **an open circuit.** It is unclear what "the transistor circuit" is meant by (a single transistor 1106 or the whole circuit of figure 11 comprising inverter). Assumed that the "transistor circuit" is the circuit of figure 11 comprises 1102, 1104, 1106 then when there are no signals applied to this circuit (open, dead) there will be no need for considering the effect of the parasitic effected at the first terminal. Clear explanation is required.

Regarding claims 9 and 10, the recitation "while sustaining **a less than equivalent increase in resistance** of the transistor circuit" is indefinite because it is unclear what it is meant by. The predetermined parasitic characteristics of the third transistor are **parasitic capacitances** that is

not related to the " **increase in resistance** of the transistor circuit". It is not clear what the "parasitic resistance" is meant by. Explanation is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2, insofar as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Huijsing et al. (US Pat. 4,678,947).

Regarding claim 1, figure 2 of Huijsing shows a transistor circuit for implementing a switch, comprising: a first switch node (T1) configured to connect to an external circuit; a second switch node (T2) configured to connect to the external circuit; a transistor device (Q0) having a first terminal electrically communicating with the first switch node, a second terminal connected to the second switch node, and a third terminal (base of Q0) configured to receive a control signal (CT) that controls the electrical connectivity between the first terminal and the second terminal; a third switch node (N1) for receiving the control signal (CT); and an impedance circuit (A1, R1, R2, 14 , A2) connected to the third switch node (N1) and the third terminal of the transistor device, the impedance circuit configured with a sufficiently high impedance (col. 4 lines 43, 44) to "reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device" by preventing the third switch node from functioning as an alternating current ground during operation of the switch. Note that the high impedance circuit (A1, R1, R2, 14, A2) isolates the input (CT) from the third switch node (N1) thus, in an AC operation, the voltage at node (N1) is not pulled to ground and the high impedance of circuit (A1, R1, R2, 14, A2) provides **a very low droop rate** thus, the effect of the parasitic capacitance that increases the slew rate of the circuit is compensated. Moreover, because the impedance circuit acts as an isolation when the input is pulled to the ground (AC operation), the base of transistor (Q0) is isolated from the ground. As a result, the parasitic

capacitances (base- emitter and base-collector) are not connected to the ground and the intrinsic parasitic capacitance of transistor (Q0) is reduced.

Claims 3 and 4, insofar as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Chiba et al. (US Pat. 5,323,063).

Regarding claims 3 and 4, figure 3 of Chiba shows a transistor circuit for implementing a switch, comprising:

a first switch node (the source of T16) configured to connect to an external circuit;

a second switch node (the drain of T16) configured to connect to the external circuit;

a transistor device (T16) having a first terminal connected to the first switch node, a second terminal connected to the second switch node, and a third terminal (G) configured to receive a control signal (IN) for controlling the electrical connectivity between the first terminal and the second terminal; and an inverter circuit (T13, T14) connected to the second terminal of the transistor device for "reducing the noise at the first terminal of the transistor device, the inverter circuit configured to reduce parasitic effects at the first terminal when the transistor circuit functions as an open circuit by providing a voltage to the second terminal when the control signal engages the transistor device". Note that when the control signal (IN) is at a low level, transistor (T16) is open (off); inverter (T13, T14) applies a high level on the gate of (T15) in order to turn (T15) on. A voltage (Vcc) is applied to the second terminal (D of T16). Inverter (T13, T14) has high input impedance thus providing **a very low droop rate.** As a result, the effect of the parasitic capacitance that increases the slew rate of the circuit is compensated. Moreover, because the inverter circuit acts as an isolation when it is not activated, the drain of transistor (T15) is isolated. As a result, the parasitic capacitances (gate-drain) are not connected to the ground and the intrinsic parasitic capacitance of transistor (T15) is reduced when (T15) is opened. Transistor (T15) is a MOS transistor.

Claims 6, 7, insofar as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Okamura (US Pat. 5,559,451).

Regarding claims 6 and 7, figure 5 of Okamura shows a transistor circuit for implementing a differential switch comprising:

a first switch node (the drain of 21) configured to connect to an external circuit;

a second switch node (the source of 22) configured to connect to the external circuit;

a first transistor device (21) having a first terminal connected to the first switch node, a second terminal, and a third terminal configured to receive a control signal (IN) that controls the electrical connectivity between the first terminal and the second terminal;

a second transistor device (22) having a first terminal connected to the second terminal of the first transistor device, a second terminal connected to the second switch node, and a third terminal configured to receive the control signal (IN); and

a third transistor device (23) having a first terminal connected to the first terminal of the first transistor device 21), a second terminal connected to the second terminal of the second transistor device (22), and a third terminal configured to receive the control signal (IN), the third transistor device configured with predetermined parasitic characteristics (inherently) that improve the effective parasitic characteristics of the transistor circuit. Note that when the third transistor (23) is turned on, its parasitic capacitances is connected in parallel with the parasitic capacitances of the first and second transistors thus, the parasitic characteristics of the transistor circuit is changed accordingly (improved). All transistors of the circuit are MOS transistors.

Regarding claim 9 and 10, because of the effect of the parallel connection of the transistors of the circuit, the equivalent resistance of the circuit is less than the resistance of the transistors and the capacitance is increased.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huijsing et al. (US Pat. 4,678,947).

Regarding claim 2, figure 2 of Huijsing includes all the limitations of claim 2 except for the limitation that the transistor device is MOSFET transistor. However, it is well known in the art that MOSFET transistors consume less power than the bipolar transistors. Therefore, it would have been obvious for those skilled in the art to replace bipolar transistor (Q0) of Huijsing with a MOSFET transistor for easy fabrication and power saving.

Response to Arguments

In page 9, first paragraph, the Applicant argues in the remarks that the circuit of Huijsing (4,678, 947) does not teach or suggest that the circuit connected to the third switch and the third terminal of the transistor device is configured with "a sufficiently high impedance to reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current ground during operation of the switch". In fact, figure 2 if Huijsing shows that transistor (Q0) is connected to an impedance of circuit (A1, R1, R2, 14, A2). In AC operation condition, the impedance circuit isolates the base of transistor (Q0) and the ground. As a result, the parasitic capacitances (base-emitter and base-collector) are not connected to the ground and the intrinsic parasitic capacitance of transistor (Q0) is reduced and this is the fact, not the result. Therefore, the rejection is proper.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-6251.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen

02-25-03

TUAN T. LAM
PRIMARY EXAMINER